AMENDMENTS TO THE SPECIFICATION

Please replace the paragraph at page 10, line 21, with the following rewritten paragraph:

3. Field and thin oxide layers are deposited, and etched to form a window for the floating gate metal contact. The metal contact is deposited, and covered with a further layer of thick oxide. When a layer of silicon diode is deposited on top of an existing layer, a solid insulator is ~~form~~ formed but with a minor systematic "crack" between the layers. The etching process leaves impurities along this interface, thus allowing a small amount of charge transport to occur along this inter-dioxide layer.

Please replace the paragraph at page 11, line 10, with the following rewritten paragraph:

~~This~~ The architectures described above are usable in both analogue and digital circuits. In digital circuits an important use would be to allow the tuning of threshold voltages of the transistors. Assuming all devices are made with leaky gate structures, the thresholds of the devices may be tuned to close to 0V allowing for much lower supply voltages. Supply voltages between 0.5 - 1 V have been demonstrated in standard high-threshold CMOS with more complicated, UV-based floating gate tuning techniques. Many different kinds of gates may be designed and it is anticipated that the area-penalty for using these devices is small. Device count is usually reduced, whilst stacked transistors may be replaced with a single transistor having dual control gates.